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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/826,179	04/04/2001	Keisuke Goto	KPM-01501	2868

26339 7590 10/07/2003

PATENT GROUP  
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EXCHANGE PLACE, 53 STATE STREET  
BOSTON, MA 02109

EXAMINER

LE, DINH THANH

ART UNIT	PAPER NUMBER
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2816

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application N .

09/826,179

Applicant(s)

GOTO ET AL.

Examiner

DINH T. LE

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 August 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-9 and 17-24 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 24 is/are allowed.
- 6) ☒ Claim(s) 1-9 and 17-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

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## **NON-FINAL REJECTION**

### **Response to Applicant's Amendment**

The rejection under 35USC 112, first paragraph, is withdrawn in view of the amendments to the claims.

The rejections over Shibayama (US 6,111,448), Jefferson (US 5,642,082) and Figure 9 of the applicant's admitted prior art are withdrawn in view of the arguments presented in the amendment

### ***Claims Rejections***

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-7, 9, 17-19 and 21-23 are rejected under 35 USC 102 (e) as being anticipated by Mnich (US ,346,839).

Mnich discloses in Figures 1-5 shows a DLL circuit comprising a phase detector (14) and a delay circuit having a variable delay section (32, Figure 2) and a fixed delay section (36, Figure 4B) for receiving a frequency variable clock signal (CLOCK) at a first node (2) to

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generate a first internal clock signal (SYNC CLOCK) at a second node (38). The delay time of the variable delay circuit (32) is adjusted by the control signals (VR, VC) based on the change of based on the frequency variable clock signal while the fixed delay (36) includes inverters (112a) having fixed delay time. Note that the variable delay circuit comprising a plurality of inverters (44, 46, 56, 58) as shown in Figure 2 and the fixed delay circuit includes a plurality of inverters as shown in Figure 4B and each output of the inverters would inherently provide a delayed output signal.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 8 and 20 are rejected under 35 USC 103 (a) as being unpatentable over Mnich (US 6,346,839) in view of Iwamoto (JP02000196444A).

Mnich discloses in Figures 1-5 a DLL circuit comprising all of the limitations of the claimed invention as discussed above but does not disclose that the delay elements of the second delay section has the same delay time as recited in claims 4 and 20 and the delay element includes an inverter and a buffer as recited in claim 8. For example, Figure 4B of Mnich shows each of the delay elements comprises an inverter (112) and a capacitor (114). Iwamoto teaches in Figure 4 a delay circuit comprising a buffer (BF41) connected between the inverters for isolating the inverters. It would have been obvious to a person having skill in the art at the time

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the invention was made to employ the buffer taught by Iwamoto for the purpose of providing an isolation between the inverters. Also, as understood by a person skill in the art, each of the delay elements of Mnich can be selectable to have a different time delay (phase shift) or the same time delay (phase shift) depending upon a particular application. Thus, selecting the delay time for the delay elements is a common practice and is considered to be a matter of a design expedient for an engineer. Lacking of showing any criticality, a skilled artisan would have been obvious to select the delay time of the delay elements of Mnich for the purpose of accommodating with the requirement a predetermined system in which the circuit of Mnich is to be used.

#### ***Allowable Subject Matter***

Claim 24 is allowable because the logic circuit s (203) in Figure 9 of the applicant's admitted prior art does not generate an enable signal in synchronism with the first internal signal and a lath signal in synchronism with the first internal clock signal.

#### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Dinh Le whose telephone number is (703) 305-3790. The examiner can normally be reached on Monday to Friday from 7:00 A.M. to 5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (703) 308-4876. The fax phone number for this Group is (703) 308-7722.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

DINH LE  
Primary Examiner

A handwritten signature in black ink, appearing to read 'Dinh Le', with a long horizontal flourish extending to the right.